REMARKS

Claims 1-4, 11-15, 21-25, and 32-43 are pending in the present application. Claims 1-43 were examined. Claims 5-10, 16-20, and 26-31 have been cancelled by amendment.

In the office action mailed May 8, 2006 (the "Office Action"), the Examiner objected to claims 10, 20, 31, and 37 based on informalities and rejected claims 1, 5, 11, 16, 21, 26, 32, 34, 36, 38, and 40 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2005/0105350 to Zimmerman (the "Zimmerman application") in view of U.S. Patent No. 6,901,494 to Zumkehr *et al.* (the "Zumkehr patent"). The Examiner further rejected claims 2-10 and 12-43 under 35 U.S.C. 103(a) as being unpatentable over the Zimmerman application in view of the Zumkehr patent, and further in view of U.S. Patent No. 6,782,435 to Garcia *et al.* (the "Garcia patent").

As previously mentioned, claims 5-10, 16-20, and 26-31 have been cancelled. The Examiner's objections and rejections to the cancelled claims is now moot.

With respect to the Examiner's objection to claim 37 based on informalities, claim 37 does not recite either phrases "the first set of data" or "the second set of data," which is the language objected to by the Examiner. Clarification of the Examiner's objection to claim 37 is requested.

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Embodiments of the present invention are directed to a memory hub having bypass circuitry that provides data bypass for a bidirectional data bus in a hub-based memory sub-system. The data bypass circuit is used to temporarily capture data passing to a distant memory hub, which allows data returning from another distant memory hub to pass through the memory hub before the captured data continues onto the distant memory hub. Thus, the data bypass circuit provides a data bypass mechanism that can be used to avoid data collisions on the bidirectional memory controller/hub interface to which the memory hub is coupled.

An example described in the present application illustrates the benefit of the data bypass circuit by describing a situation where read data can be returned from a first memory module 130b although outbound write data to be written to a second module 130c has already been provided by the memory hub controller 128. The outbound write data is captured by the data bypass circuit of the memory hub 140a to clear the bidirectional data path and allow read data to return to the memory hub controller 128 from the first memory module 130b without colliding with the outbound write data. After the read data passes through the memory hub 140a, the outbound write data is recoupled to the bidirectional data path to continue on its way to the memory module 130c to be written into the memory device 148c. *See* paragraph 25 and Figure 4 of the present application (referencing U.S. Patent application Publication No. 2005/0177695 to Larson *et al.*).

In contrast to the present application, the Zimmerman application is directed to a memory test mechanism for buffered-memory-module memory subsystems. As described in the Zimmerman application, it is desirable to provide testing and evaluation of individual memory modules and individual module-to-module memory channels independent of the host and host memory channel. A memory module buffer (MMB) on each of the buffered memory modules is coupled to a SMBus 160 to provide a separate channel to allow testing independent of a memory controller and host memory channel. Commands can be issued directly to one of the memory modules using the SMBus 160 to bypass the host memory channel 112 and any intervening module-to-module memory channels and memory modules. As illustrated in the Zimmerman application, the memory channels have separate uni-directional data paths for "northbound" and "southbound" data. *See* Figures 2-8. Figures 4 and 5 illustrate the MMB 200 having connections for coupling to both a northbound data path and a separate southbound data path. In the arrangement described and shown in the Zimmerman application, collision between incoming read data and outbound write data is avoided without the need for a bypass circuit because the read data and write data are transferred on separate data paths, namely, the northbound data path and the southbound data path.

The Examiner further cites the Zumkehr patent for teaching memory controller hub circuits, including a write buffer that can defer a write data transfer temporarily stored in the write buffer, while allowing the read data command from an SDRAM device to be transferred

from SDRAM devices to the memory controller. *See* the Office Action at page 3. According to the Examiner, it would have been obvious to include the memory controller hub circuits and method of Zumkehr in the Zimmerman system. *See id.*

The Zumkehr patent is directed to a memory control unit 111 having a memory controller 210 of a first memory protocol and a translator hub 220 that translates control and data signals issued in the first protocol into a second memory protocol to be provided to memory devices 161 operating according to the second memory protocol. In the example described in the Zumkehr patent, the memory controller 210 is a RAMBUS memory controller providing control and data signals according to a RAMBUS protocol, and the memory devices 161 are SDRAM memory devices operating according to a SDRAM protocol. The translator hub 220 addresses the poor bus utilization problems identified in the Zumkehr patent that are associated with conventional interfaces and translators. Namely, RAMBUS memory controllers defer write data transfers on a write command until a read latency (of a previous read operation) is met. A conventional translator does not adjust for this deferral, and consequently, issuance of write commands to the SDRAM memory devices is delayed until the write data is finally sent from the RAMBUS memory controller. *See* Figure 5A and col. 2, lines 10-25 and col. 6, lines 7-52.

An example of a translator hub according to the teachings of the Zumkehr patent is shown in Figure 3. The translator hub 220 includes a write buffer 330 in which a write command and associated write data are stored for provision to the SDRAM memory devices at a later time. Operation of the translator hub, and the write buffer 330, is described in more detail in the Zumkehr patent with reference to Figure 5B. The write buffer 330 stores a previous write command 522B and associated data 525B to be provided to the memory devices (represented in Figure 5B by the "command from hub to SDRAM" and "SDRAM data bus") in response to the translator hub 220 receiving a new write command 520B from the RAMBUS memory controller. The new write command 520B is stored in the write buffer 330 as the previous write command 522B and associated write data 525B are provided to the memory devices. Figure 7 illustrates a flow diagram for operation of the translator hub 220 and the write buffer 330.

By storing a previous write command 522B and associated write data 525B, and providing the same to the memory devices in response to receiving a new write command, the previous write command 522B and data 525B can be provided to the memory devices without

waiting for the write data 527B of the new write command 520B. As a result, bus utilization between the memory devices, through the translator hub 220 and back to the RAMBUS memory controller is improved. When the write data 527B for the new write command 520B is finally issued by the RAMBUS memory controller to the translator 220, it is stored in the write buffer 330, where it and the new write command 520B are held until receipt of the next write command.

As previously mentioned, claims 1, 11, 21, 32, 36, and 40 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Zimmerman application in view of the Zumkehr patent.

Claim 1 recites a memory hub that includes, among other things, a data path having a direct data path and a bypass data path, the bypass data path having a write bypass circuit coupled to the direct data path operable to couple write data on the direct data path and temporarily store the write data to allow read data to be transferred through the direct data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred through the direct data path. Claim 11 is directed to a memory module having a memory hub similar to that of claim 1, and claim 21 is directed to a processor-based system including a memory module having a memory hub similar to that of claim 1.

Claims 1, 11, and 21 are patentable over the Zimmerman application in view of the Zumkehr patent because the combined teachings fail to teach or suggest the combination of limitations recited by the respective claims. For example, neither the Zimmerman application or Zumkehr patent disclose a data path having a direct data path and a bypass data path as recited in the claims. As previously discussed, the Zimmerman application describes a memory subsystem having memory channels having separate northbound and southbound data paths to couple the MMBs together. Claims 1, 11, and 21 recite that the memory hub is configured to be coupled to a bidirectional data bus, that is, one on which the signal lines can be used to transfer both read and write data.

As for the Zumkehr patent, the translator hub 220 includes a write buffer 330. However, the translator hub 220 does not include a data path having both a direct data path and a bypass data path as recited in claims 1, 11, and 21. As described in the Zumkehr patent, and as

previously discussed, write data provided by the RAMBUS memory controller to the SDRAM devices by way of the translator hub 220 is stored in the write buffers 330 and not provided to the SDRAM devices until receipt of a subsequent write command. Write data is not provided directly to the SDRAM devices so that the translator hub 220 is not forced to wait until the RAMBUS memory controller finally sends the write data for a current write command before providing write data (from a previous write command) to the SDRAM devices. In Zumkehr, the write data from a previous write command is transferred to the SDRAM devices while the translator hub 220 waits for the write data of a new write command to be provided by the RAMBUS memory controller. There is not a direct data path for the write data to be provided to the SDRAM devices, as there is in the data path recited in claims 1, 11, and 21.

Claims 32, 36, and 40 are similarly patentable over the Zimmerman application in view of the Zumkehr patent. Claims 32, 36, and 40 recite methods for writing data or executing memory commands in a memory system coupled to a bidirectional memory bus. The claims as amended recite a combination of limitations that are not taught or suggested by the teachings of the Zimmerman application and the Zumkehr patent. For example, with reference to claim 32, the recited method includes coupling the write data to a register in the memory system for temporary storage of the write data to allow the read data to be returned on the bidirectional data bus after the write data is provided to the same and before the write data has been written. The Zimmerman application, which is directed to a test mechanism for memory modules, does not describe the coupling of write data and the return of read data in the manner recited. As for the Zumkehr patent, write data for a write command issued after a read data is not buffered to allow the read data to be returned without data collision. As previously discussed, the Zumkehr patent describes buffering write data from a previous write command, which is then provided to the SDRAM devices upon receipt of a new write command. In Figure 5B, the write data 527B of the write command 520B (issued after the read command 501B) is not buffered to allow the read data 510B to be returned. The buffered write data 525B is associated with the previous write command 522B, which is issued prior to the read command 501B.

The difference between the Zumkehr patent and claims 32, 36, and 40 is due to the different purposes of buffering write data. As previously discussed for embodiments of the present invention, the bypass circuit is provided to avoid data collision between data heading in

opposite directions on the bidirectional data path, for example, between outbound write data issued after a read command and read data returning on the bidirectional data path in response to the same read command. The Zumkehr patent, in contrast, includes the write buffers 330 in the translator hub 220 so that write data (from a previous write command) can be provided to the SDRAM device during the time the translator hub 220 is waiting for write data for a new write command. The write data is buffered so that it can be provided at a later time, and not for the purpose of clearing the data path for return data, before the write data is recoupled to the data path to continue on its way to be written.

For the foregoing reasons, claims 1, 11, 21, 32, 36, and 40 are patentable over the Zimmerman application in view of the Zumkehr patent. Claim 34, which depends on claim 32, and claim 38, which depends from claim 36, are similarly patentable based on their dependency from a respective allowable base claim. Therefore, the rejection of claims 1, 11, 21, 32, 34, 36, 38, and 40 under 35 U.S.C. 103(a) should be withdrawn.

As previously mentioned, claims 2-4, 12-15, 21-25, and 32-43 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Zimmerman application in view of the Zumkehr patent, and further in view of the Garcia patent.

The Garcia patent has been cited by the Examiner for teaching a multiplexer, a bypass selection signal, and a register to temporarily store write data being received. See the Office Action at page 4. Even if it is assumed for the sake of argument that the Examiner's characterization of the Garcia patent is accurate, it fails to make up for the deficiencies of the Zimmerman application and the Zumkehr patent, as previously discussed.

For the foregoing reasons, claims 2-4, 12-15, 21-25, and 32-43 are patentable over the Zimmerman application in view of the Zumkehr patent, and further in view of the Garcia patent, and therefore, the rejection of claims 2-4, 12-15, 21-25, and 32-43 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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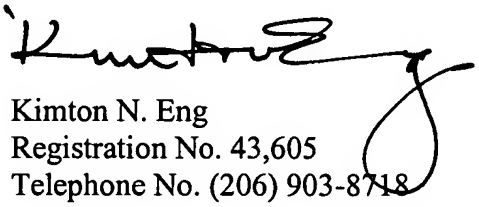

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